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Placement Algorithms and Logic on Logic (LOL) 3D Integration

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Abstract

In the present study, three algorithms for placement of standard 3D cells have been analyzed. These algorithms are 3D placement using 2D placement devices, real 3D analytic placement using mPL, and 3D placement simultaneously using 2D and mPL placements. These algorithms are used to place three case studies in a real face-to-face 3D process. These three case studies include: two-point FFT butterfly processing element known as PE, advanced embedded series or AES, and wireless decoding with multiple input and multiple output (MIMO). Afterwards, displacements are compared with 2D placements regarding performance and power consumption. Then, using this technology, i.e. face-to-face 3D integration with micro bump along with three placement algorithms, timer speeds of AES and PE modules are respectively increased as 3.15% and 6.22% while their power consumption are reduced to 6.2% and 9.12%, respectively.

Keywords: Placemen, mPL, 3D Integration, 3D Placement

1. Introduction

The present study deals with this question, “To what extent does applying real 3D affect devices in combining LOL 3D designs?” In fact, using such devices reduces wire length remarkably. Wire length reduction resulted from LOL integration causes power consumption to decrease and performance to increase. Improving this criterion is the purpose of the present study. In the current research, three case studies have been used to investigate power consumption and performance of 3D LOL integration. These three case studies are: two-point FFT butterfly processing element known as PE, advanced embedded series or AES, and wireless decoding with multiple input and multiple output (MIMO). In our view, these three studies provide different designs. Butterfly processing element is a weak design with a too long route which passes through a multiplier and two adders. AES module is adopted from an open core repository and its route is shorter than that of PE. Wireless decoding design of MIMO has a large number of flip-flops that record movements. These case studies are conducted in 3D IC 130 nm Tezzaron’s process which is explained in section 3. In the present study, three different 3D placement algorithms are compared with a 2D placement algorithm. Placement algorithms include 3D placement using 2D placement devices, real 3D analytic placement using mPL, and 3D placement simultaneously using 2D and mPL placements, which are explained in sections IV-IV, IV-B, D-C, respectively.

2. Review of the Literature

Other studies have been conducted on the issue of standard 3D cell placement including Hentschke*et al* [2], Deng *et al* [3], and Cong *et al* [4]. In the study conducted by Hentschke*et al*, a second-rate placement algorithm is introduced to place standard cells, which reduces 32% of the total length of the wire by creating 5 rows on ISPD of the year 2004. Deng *et al* have showed that 4.21% of the total length of the wire is resulted from standard 3D cell. In the study conducted by Cong *et al*, transformation method has been used to reach 3D placement solutions by creating balance between TSV and wire length out of an improved 2D placement method. All of these studies have focused on reducing wire length which is regarded as an important criterion. This criterion; however, cannot illustrate a general image because pinpointing improvement of performance and power consumption directly is a difficult undertaking. There is a detailed study on 3D physical algorithms in [5].

3. 3D Integration Technology

Potential advantages of using 3D placing and routing in a digital system are totally reliant on involved 3D technology parameters. There are four parameters that have most effect on the result including Via effect in micrometers, a small hole beside which 2 Vias are located side by side (and in micrometers), metal layers which are blocked by a Via, looseness and firmness of a Via. Table I shows these three 3D Via parameters.[6]

via	footprint	pitch	grid	block
MIT laser drilled TSV	3.2 by 3.2	4.1	NO	all
Tezzaron Super contact TSV	1.3 by 1.3	1.67	NO	all
Tezzaron copper microbump	5.2 by 5.2	6.0	YES	NONE

Table I. Parameters of 3D vias

Parameters of 3D IC 130 nm Tezzaron'sprocess [7], [8], and [9] are used in placements. The advantage of this process in that communication between the rows does not result in any blockage of the routes because the design of the micro bumps is face-to-face (the left figure of Diagram 1) as opposed to TSVs where the communication is between the rows.

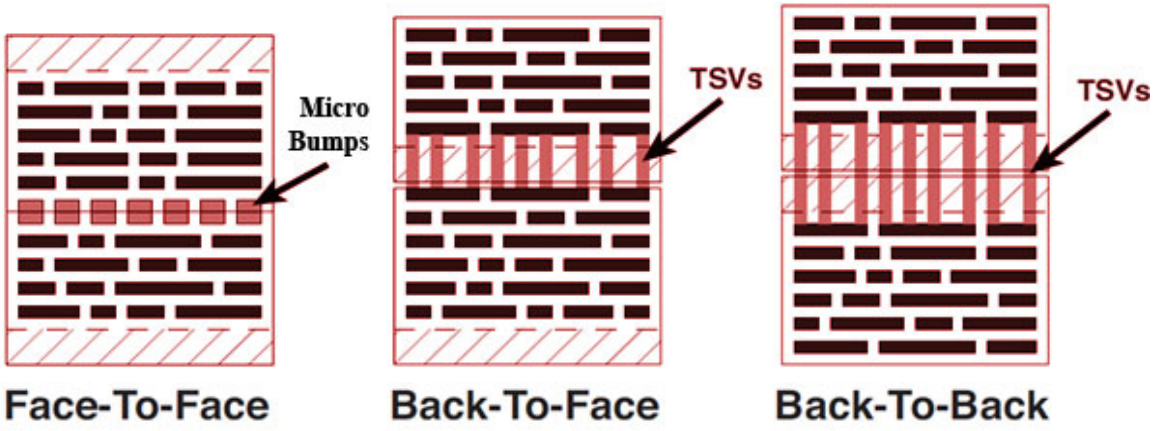

Fig. 1. The three different stacking orientations, with the interconnect and substrate shown [9].

4. 3D Placement

In this section, three methods of 3D placement are discussed. These methods are 3D placement using 2D placement devices, real 3D analytic placement using mPL, and 3D placement simultaneously using 2D and mPL placements. In addition, these methods are compared to 2D placement.

4.1. 2D Placement using Traditional Devices

As its name suggests, 2D placement using off-the-shelf devices is a traditional placement that is conducted through trading devices. The trading device which is applied in placing and routing is cadence encounter. Since a single device is used in placing and routing, a fair comparison between 2D and 3D placements is needed.

4.2. 3D Placement using Traditional 2D Devices

The first placement algorithm to be investigated is much similar to 2D placement because investigating 3D placement is one through two separate 2D placers and traditional trading devices, which acts as follow: first, the netlist design is presented through a hypergraph where the nodes and the hyperedges are consistent with standard cells and networks connecting these cells, respectively. Afterwards, the hypergraph is divided into two equal halves each of which has the minimum edge possible. This division is carried out through hMetis |10| and its balance is gained by reducing the number of the edges. This is done so that the balance does not decline as a result of imbalance between the rows. Then, placement through cadence encounter is completed this way: the first 2D row is placed in input and output pins without any restriction. Then, this placement is applied in 3D Via transfer. After that, the first row is used to restrict replacement. Then placement of the second row is conducted.

4.3. Real 3D Analytic Placement using mPL

This placement is conducted by using the analytic 3D placement of 3DMpl |11|. This analytic placement conducts 3D placement through a non-linear programing (NLP). Variables are horizontal placers of |x, y| for each cell and vertical placer of |z| for each row. Transferring the middle row makes placement between the side rows possible and finally the problem will be solved. Weight of 3D Vias is assigned as the small amount of (1.0) for placement case studies, which leads to an increase in the number of 3D Vias.

4.4. 3D Placement Simultaneously using 2D and mPL Placements

This quasi-3D placement is also carried out with mPL-3D and conducted in a way that it is a combination between placements in section IV-B and IV-C but it uses less Vias compared to that of section IV-C. This algorithm of transferring the right row like section IV-B is carried out using hMetis. However, instead of applying two separate 2D placements, mPL-3D with transfer of (Z) row is conducted. An only horizontal placer of (x, y) is considered as the variable. Here, placement of IV-B is also improved because each row directly affects the placement of the other rows.

5. 3D Routing

In order to investigate power consumption and LOL 3D integration performance, cell 3D routing should be completed. Fortunately, the difference between 2D and 3D routing is lesser than that of 2D and 3D placement because multi-facet metal layers in 3D routing create a 3D structure which is similar to that of 2D wiring. The method used here includes dividing 3D routing problem into 2D separate routing problems which can be solved through traditional 2D routing devices. This method is explained through a 3D transfer algorithm in section V-A.

5.1. 3D Via Transfer

In this section, 3D Via transfer is described. This algorithm was first introduced by Thorolfsson*et al* and applied for all three algorithms of 3D placement. This algorithm is created based on E algorithm and acts as follow: first, a plate was created which was tangent to 3D Via plate. Every wire that goes through the rows is transferred to a place that was nearest to the wire terminal of the timer. After initial transfer, movement in each place with more than one inter-row wire is conducted. Movement is carried out from places with the maximum number of wires to those with the minimum number of wires. Movement is carried out this way: the shortest route from a place to a free place is found using Lee's algorithm. Contents of each place are transferred to the free place through the route, which results in inter-row wire length reduction. Movement continues until no place contains more than one inter-row wire.

The algorithm is presented as follows.

***Input**: Location of cells that connect to 3D vias*
***Output**: The 3D via assignmen*
Assign Every Inter Tier Signal to nearest grid square();
For each** Grid square $i\ \ j > 1$ **Do
IF** 3D vias assigned to $i\ \ j > 1$ **then
While** 3D vias assigned to $i\ \ j > 1$ **Do
K=shortest path to free grid square();
For each** 3D via on path k **Do
Shift 3D via along path();
End
End
End
End

6. Results

The results of these three case studies are as follows. Each of the case studies is combined with a netlist using Synopsys design compiler and is transferred to the cadence encounter through an encounter or mPL-3D depending on the type of the placement algorithm. Number of 3D Vias for each placement algorithm is varying. Real 3D analytic placement algorithms use more 3D Vias (and less wire length) compared to the other two placement algorithms. Table II presents placers used in each case study.

	3D vias used	3D via available	Util
PE 3D seq.	395	6323	5.9
PE 3D sim.	325	5900	4.9
PE 3D true	1434	5900	19.2
AES 3D seq.	243	20.1	5.1
MIMO 3D seq.	2565	8116	31

Table II . The 3D via utilization numbers the 3D placement algorithms for the different case studies.

In each placer, cells that use time signals are kept in the same row, which helps the design to be resistant against inconsistencies of the process. After placement, time tree combination is conducted using cadence encounter. After routing, the inter-link noises within the SPEF file and the total wire length are assessed. Then, SPEF file and prime time are read this is the time when the maximum time length and power consumption are determined based on noises of the mentioned file. Due to time limitations, real ordered and 3D placement will not be completed. The numeric results of the placements are given in Table III; and then improvement percentage of 2D placement is presented in Table IV.

	Ototalwire length(mm)	Max frequency (mhz)	Parasitic power (mw)	Total power (mw)
PE 2D	577.0	31.51	1.693	5.874
PE 3D seq.	477.2	32.87	1.417	5.593
PE 3D sim.	467.3	35.71	1.295	4.414
PE 3D true	563.7	37.75	1.001	5.203
AES 2D	457.6	249.64	4.9	37.1
AES 3D seq.	432.9	287.01	4.2	36.1
MIMO 2D	306.7	222.22	5.2	42.3
MIMO 3D seq.	984.1	2.63.08	4.4	43.1

Table III. Results from the four placement algorithms,with all the power measurement done at the maximum clock speed of the 3D placement.

	Ototal wire length(change %)	Max frequency (change %)	Parasitic power (change %)	Total power(change %)
PE 3D seq.	-16.9	+6.9	-16.8	-5.8
PE 3D sim.	-17.3	+17.1	-28.8	-8.8
PE 3D true	-22.0	21.9	-46.8	-13.4
AES 3D seq.	-8.0	+16.1	20.1	3.1
MIMO 3D seq.	+221.1	+18.2	-33.8	-6.2

Table IV. Results from the four placement algorithms,with all the power measurement done at the maximum clock speed of the 2D placement.

In both tables, PE, AES, and MIMO are related to FFT processing element, advanced embedded series, and wireless decoding, respectively. Moreover, an image of placing and routing in case study of AES about 2D placement and ordered 3D placement upwards and downwards are presented in diagrams 2, 3, and 4, respectively.

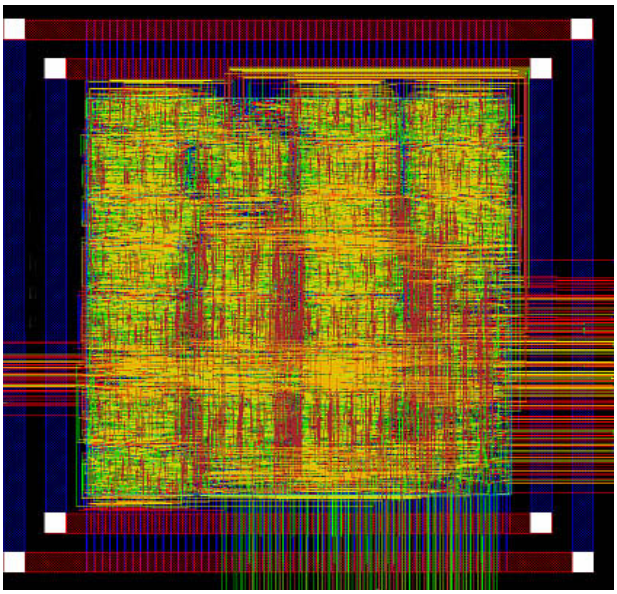

Fig. 2A picture of the 2D placed AES module.

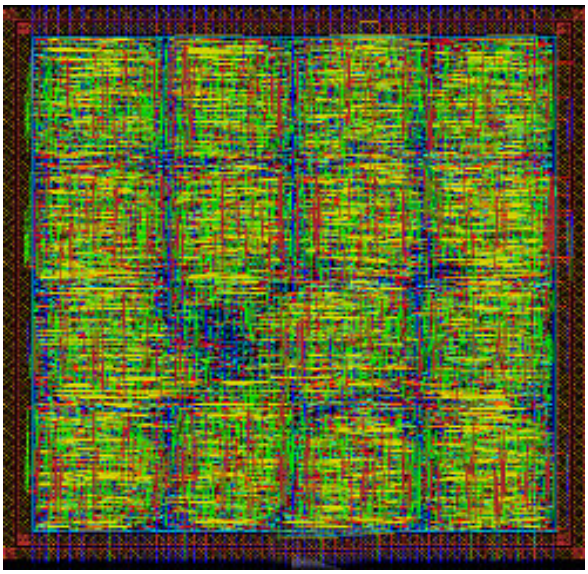

Fig. 3 A picture of the top of the 3D sequentially placed AES module.

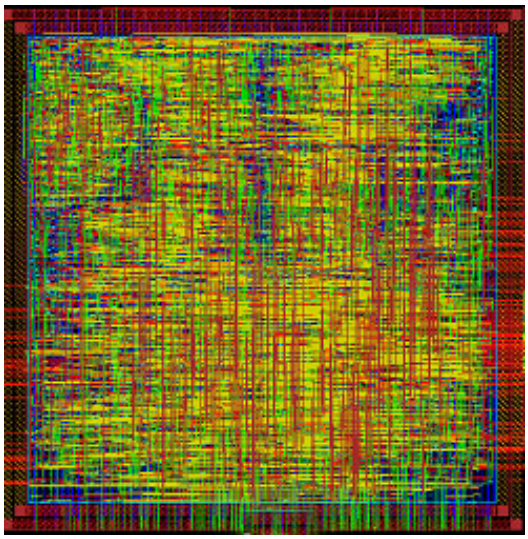

Fig. 4. A picture of the bottom of the 3D sequentially placed AES module.

7. Conclusion

The present study showed that using LOL integration can improve maximum time frequency up to 6.22% and power consumption up to 9.12% indifferent digital circuits. Exerting more effort and applying the present 2D devices this improvement is practical as it has been proved about 3D placement by using traditional 2D placement algorithms. Moreover, using face-to-face integral improves the result. Micro bumps do not block the route as opposed to TSVs. Finally, these results are reliant on this fact that a specific number of the cells have enough 3D communication.

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